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EXAMINER	
WOZNIAK, JAMES S	
ART UNIT	**PAPER NUMBER**
2655	

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/898,282	PRINTZ ET AL.	
	Examiner	Art Unit	
	James S. Wozniak	2655	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 7/26/2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 3/1/2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Response to Amendment

1. In response to the office action from 3/25/04, the applicant has submitted an amendment, filed 7/26/04, amending claims 1, 17, 18, and 20, while arguing to traverse the art rejection based on the limitation regarding a uniformly accessible language model cache mapped to a common address space *(Amendment, Page 9)*. Applicant's arguments have been fully considered, however the previous rejection, altered only with regards to the amended claims and without the addition of any further prior art, is maintained due to the reasons listed below in the response to arguments.

Response to Arguments

2. Applicant's arguments have been fully considered but they are not persuasive for the following reasons:

- With respect to **Claim 1**, the applicant argues that Fisher et al (U.S. Patent: 6,061,653) fails to teach the use of multiple memory processors that can each uniformly access a language model cache mapped to a common address space *(Amendment, Page 9)*, however Fisher discloses a process independent model storage area, which is a functional equivalent of a uniformly accessible language model cache *(Col. 6, Lines 45-60)*. Although speech models are separated based on process dependency to

create two storage areas (process dependent and independent) and the dependent model storage area is not uniformly accessible, the speech models within the process independent storage area are uniformly accessible by all DSPs (Col. 6, Lines 49-52). This sharing of speech models by multiple DSPs is further evidenced in the background of the invention, which states that the invention is related to using shared speech models to improve speech recognition efficiency *(Col. 1, Lines 16-19)*. Thus, Fisher et al teaches the claimed uniformly accessible language model cache and the rejection of claims 1 is maintained.

- Dependent **claims 2-16, 19, and 21** are argued as further limiting their parent claims *(Amendment, Page 10)*. Thus, since the rejection of claims 1, 17, 18, and 20 is maintained, Claims 2-16, 19, and 21 remain rejected.
- With respect to **Claims 17, 18, and 20**, the applicant argues that Fisher fails to teach the use of multiple memory processors that can each uniformly access a language model cache mapped to a common address space *(Amendment, Page 10)*, however Fisher teaches a similar feature with respect to Claim 1 as noted above. Thus, for the reasons noted above with respect to Claim 1, the rejection of claims 17, 18, and 20 is maintained.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-3 and 15** are rejected under 35 U.S.C. 102(e) as being anticipated by Fisher et al *(U.S. Patent: 6,061,653)*.

With respect to **Claim 1**, Fisher discloses:

A speech processing board comprising:

Multiple processor modules *(plurality of DSPs, Col. 3, Lines 14-15, and Fig. 1, Element 18)*, each said processor module having an associated local memory *(internal memory, Col. 3, Lines 51-53)*, each said processor module hosting at least one instance of a speech application task *(DSP speech task management function, Col. 3, Lines 59-61)*;

A storage system for storing speech task data, said storage system comprising a language model cache mapped to a common address and uniformly accessible by each said processor module and said speech task data comprising language models and finite state grammars *(database containing speaker dependent and independent models constrained by a digit grammar, Col. 3, Lines 45-47 and Col. 4, Lines 1-5, and process independent model storage area, Col. 6, Lines 45-60)*;

A local communications bus communicatively linking each said processor module through which each said processor module can exchange speech task data with said storage system (resource bus, Fig. 2, Element 32, and Col. 3, Lines 47-49); and,

A communications bridge to a host system, said communications bridge providing an interface to said local communications bus through which data can be exchanged between said processor modules and said host system *(bus interface, Fig. 1, and Col. 3, Lines 12-15)*.

With respect to **Claim 2**, Fisher recites:

A speech processing board, wherein each said processor module comprises:

A central processing unit (CPU) core having at least one memory cache that can be accessed by said CPU core *(host level application containing a database, Col. 3, Lines 43-47 and host processor, Fig. 1, Element 16)*;

A processor bridge communicatively linking said CPU core to said local communications *bus (bus interface, Col. 3, Lines 12-15 and Fig. 1)*; and

A memory controller through which said CPU core can access said local memory, said memory controller linked to said CPU core through a processor local bus *(resource bus that allows a host processor to access a database, Col. 3, Lines 43-49)*.

With respect to **Claim 3**, Fisher discloses:

A speech processing board, further comprising a language model cache disposed in said local memory *(database containing speaker dependent and independent models, Col. 3, Lines 45-47)*.

With respect to **Claim 15**, Fisher shows:

A speech processing board, wherein said host system is a CT media services system *(media server featuring computer-based processing for a telephone application, Fig. 1)*.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher et al.

With respect to **Claim 4**, Fisher teaches the speech processing device containing multiple processors capable of accessing a uniformly accessible language model and grammar database through a communications bus as applied to Claim 1. Fisher does not specifically disclose that the grammar in the database is stored in a table as recited in Claim 4, however it would have been obvious to one of ordinary skill in the art, at the time of invention, to implement the well-known method of grammar storage in a table in order to better classify grammar rules, and thus simplify the processing of grammar applied to input speech.

7. **Claims 5-10, 12-14, and 17-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher et al in view of Walsh *(U.S. Patent: 6,539,087)*.

With respect to **Claim 5**, Fisher recites:

A fixed storage device accessible by said processor modules through said communications bridge, wherein said fixed storage device stores active language models and finite state grammars used by said speech application tasks hosted by said processor modules *(database containing speaker dependent and independent models constrained by a digit grammar, Col. 3, Lines 45-49 and Col. 4, Lines 1-5)*;

A commonly addressed language model cache, said language model cache storing at least one image of a language model stored in said fixed storage device, each said processor module accessing said language model cache through said communications bridge at a common address (*database containing speaker dependent and independent models, Col. 3, Lines 45-47, contained in a host processor, Fig. 2, Element 30, that is accessible by all DSPs through a communications bus, and Col. 6, Lines 45-60)*;

Wherein said language model cache stores at least one image of a language model, and wherein each said processor module accesses said language model cache through said communications bridge *(language model stored in a process independent storage area, Col. 6, Lines 45-60, and bus interface, Col. 3, Lines 12-15 and Fig. 1).*

Fisher does not teach the use of a boot memory, however Walsh discloses:

A boot memory storing initialization code, said boot memory communicatively linked to said processor modules through said communications bridge, each said processor module accessing said boot memory during an initial power-on sequence *(RAM*

and ROM accessible via a communications bridge and capable of storing boot data accessible from a host system, Col. 3, Lines 12-25).

Fisher and Walsh are analogous art because they are from a similar field of endeavor in speech processing in a network featuring multiple speech processing modules. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to combine the boot memory accessible via a network bridge as taught by Walsh with the speech processing device containing multiple processors capable of uniformly accessing a language model and grammar database through a communications bus as recited by Fisher to allow for an increase in ease of use by eliminating the need to configure the system upon power-up. Therefore, it would have been obvious to combine Walsh with Fisher for the benefit of obtaining a speech processing network capable of retaining its previous configuration upon power-up, to obtain the invention as specified in Claim 5.

With respect to **Claim 6**, Fisher teaches a communications bus for use with a host processor and a plurality of DSPs. Fisher does not specifically disclose that this communications is a PCI bus, however Walsh recites:

A speech processing board, wherein said local communications bus is a PCI bus *(use of a PCI bus as a means of connecting DSP cards with a host processor (Col. 3, Lines 41-43).*

Fisher and Walsh are analogous art because they are from a similar field of endeavor in speech processing in a network featuring multiple speech processing modules. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to combine the use of a PCI bus as taught by Walsh with the

communications bus for use with a host processor and a plurality of DSPs as recited by Fisher to provide for further device use in a wide variety of speech processing environments that require a PCI bus. Therefore, it would have been obvious to combine Walsh with Fisher for the benefit of obtaining a speech processing network capable of communicating over a PCI bus, to obtain the invention as specified in Claim 6.

With respect to **Claims 7 and 8**, Fisher teaches a communications bus for use with a host processor and a plurality of DSPs. Fisher does not specifically disclose: a 64-bit, 133MHz PCI communication bus as recited in Claim 7 or a 64-bit, 66MHz PCI communication bus as recited in Claim 8, however Walsh suggests:

The PCI bus as applied to Claim 6 in combination with the configuration, well known to one skilled in the art of 64-bit, 133MHz and 64-bit, 66MHz PCI buses. Thus it would have been obvious to one skilled in the art, at the time of invention, to increase system compatibility by allowing for the option to choose between various PCI bus types, specifically those common values as recited in Claims 7 and 8.

With respect to **Claim 9**, Fisher discloses the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus as applied to Claim 1. Fisher does not specifically disclose an interface implemented by using a PCI-to-PCI bridge and a further interface to an H.1x0 bus, however Walsh discloses:

A speech processing board, wherein said communications bridge comprises a PCI-to-PCI bridge having a PCI interface to said host system and an interface to an H.1.times.0 bus *(additional bus connecting network interface cards, connected to a host, Col. 2, Lines 57-58, to DSP units in the form of an H.110 bus, Col. 2, Lines 40-42).*

Fisher and Walsh are analogous art because they are from a similar field of endeavor in speech processing in a network featuring multiple speech processing modules. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to combine the use of a H.110 bus as disclosed by Walsh with the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus as recited by Fisher to provide for a greater degree of compatibility with the known protocols and hardware specifications mentioned by Walsh (Col. 2, Lines 42-48). Also, it would have been obvious to one of ordinary skill in the art, at the time of invention, that the bus interface taught by Fisher, as applied to Claim 1, could be a PCI-to-PCI interface, since in order for the host to communicate with the PCI bus taught by Walsh, a PCI-to-PCI interface would need to be implemented. Therefore, it would have been obvious to combine Walsh with Fisher for the benefit of obtaining a more compatible speech processing network, to obtain the invention as specified in Claim 9.

With respect to **Claim 10**, Fisher teaches the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus as applied to Claim 1. Fisher does not teach the ability to manage message communications between the processing board and host system, however Walsh discloses:

A speech processing board, wherein said communications bridge further comprises a processing element for managing message communications between the speech processing board and said host system according to a messaging protocol provided by said host system *(communication bus connected to a host system, for*

interfacing with various protocol specifications, Fig 2, Element 122, Col. 2, Lines 42-48).

Fisher and Walsh are analogous art because they are from a similar field of endeavor in speech processing in a network featuring multiple speech processing modules. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to combine the host system capable of being connected to various messaging protocol devices as disclosed by Walsh with the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus as recited by Fisher to provide for a greater degree of compatibility with protocols and hardware specifications *(Walsh, Col. 2, Lines 42-48)*. Therefore, it would have been obvious to combine Walsh with Fisher for the benefit of obtaining a more compatible speech processing network, to obtain the invention as specified in Claim 10.

With respect to **Claim 12**, Fisher teaches the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus as applied to Claim 1. Fisher does not specifically teach an audio channel allowing the exchange of data between modules, however, Walsh discloses:

A speech processing board, further comprising a serial audio channel communicatively linking said processor modules to said communications bridge, said serial audio channel providing a medium upon which audio data can be exchanged between individual processor modules and said communications bridge *(DSP unit having*

a bridge for connecting to a host via a communications bus, Col. 3, Lines 12-15, and even audio data distribution among DSP cards, Col. 4, Lines 26-28).

Fisher and Walsh are analogous art because they are from a similar field of endeavor in speech processing in a network featuring multiple speech processing modules. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to combine the communications bus for distributing audio data and linking DSPs to a host processor via a bridge as taught by Walsh with the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus as taught by Fisher to improve processing efficiency of a speech processing board by allowing the DSPs to share processing tasks. Therefore, it would have been obvious to combine Walsh with Fisher for the benefit of obtaining a more efficient speech processing board by allowing for the ability to share processing tasks among multiple DSPs, to obtain the invention as specified in Claim 12.

With respect to **Claim 13**, Fisher teaches the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus as applied to Claim 1. Fisher does not specifically teach an audio processor that stores and distributes audio data, however Walsh suggests:

A speech processing board, further comprising an audio stream processor coupled to said communications bridge, said audio stream processor configured to extract audio information received in said communications bridge, store said extracted audio information and distribute said audio information over said serial audio channel to selected ones of said processor modules based on hosted instances of speech applications

in each said processor *module (host processor connected to a communications bus, Col. 3, Lines 12-15, for receiving and distributing audio data to appropriate DSP resources, Col. 4, Lines 16-28 and a memory accessible by a host processor, Col. 3, Lines 18-25).*

Fisher and Walsh are analogous art because they are from a similar field of endeavor in speech processing in a network featuring multiple speech processing modules. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to combine the use of a host processor to store and distribute audio processing data amongst multiple DSPs as taught by Walsh with the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus as taught by Fisher to increase processing efficiency by allowing a host processor to access required data through a memory and distributing audio data to DSPs configured to handle a specific audio processing task, thus reducing necessary memory and increasing processing speed. Therefore, it would have been obvious to combine Walsh with Fisher for the benefit of obtaining a more efficient speech processing board by distributing audio data to specific DSPs, to obtain the invention as specified in Claim 13.

With respect to **Claim 14**, Fisher teaches the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus, and featuring an audio communications channel as applied to Claim 12. Fischer does not teach an Ethernet switch as recited in Claim 14, however Walsh discloses:

A speech processing board, further comprising an ethernet switch coupled to said communications bridge, said ethernet switch configured to transmit and receive

packetized audio information to and from an external network *(switching unit (Fig. 1, Element 104) connected to the communication ports of the network interface cards that allows the host to communicate with further DSP units (Col. 2-3, Lines 63-67, 1-6).*

Fisher and Walsh are analogous art because they are from a similar field of endeavor in speech processing in a network featuring multiple speech processing modules. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to combine the switching unit as disclosed by Walsh with the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus, and featuring an audio communications channel as recited by Fisher to provide an the option of interfacing with multiple DSP instances. Therefore, it would have been obvious to combine Walsh with Fisher for the benefit of obtaining a more compatible and configurable speech processing network, to obtain the invention as specified in Claim 14.

With respect to **Claim 17**, Fisher teaches the speech processing device containing multiple processors capable of accessing a uniformly accessible language model and grammar database through a communications bus as applied to Claim 1. Fisher does not teach the PCI-to-PCI Bridge, drive controller, and boot memory as recited in Claim 17, however Walsh discloses:

A speech processing board comprising: multiple processor modules in the speech processing board; a PCI-to-PCI bridge interfacing said local PCI interface to a host CT system), said bridge comprising interfaces to an H.1.times.0 bus and a PCI bus; a local PCI interface linking each said processor module to said PCI-to-PCI bridge *(cPCI bridge, H.110 bus, Col. 3, Lines 4-34)*;

A fixed storage communicatively linked to said PCI-to-PCI bridge and accessible by said processor modules through a drive controller *(host and DSP resource accessible memory, Col. 3, Lines 15-25)*;

A boot memory communicatively linked to said bridge, said boot memory storing initialization code *(boot memory, Col. 3, Lines 15-25)*.

Fisher and Walsh are analogous art because they are from a similar field of endeavor in speech processing in a network featuring multiple speech processing modules. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to combine the use of a PCI bridge with the speech processing device containing multiple processors capable of accessing a uniformly accessible language model and grammar database through a communications bus as recited by Fisher to provide for further device use in a wide variety of speech processing environments that require a PCI interconnectivity. Also, it would have been obvious to one of ordinary skill in the art, at the time of invention, that the bus interface taught by Fisher, as applied to Claim 1, could be a PCI-to-PCI interface, since in order for the host to communicate with the PCI bus taught by Walsh, a PCI-to-PCI interface would need to be implemented. Therefore, it would have been obvious to combine Walsh with Fisher for the benefit of obtaining a speech processing network capable of communicating over a PCI bus, to obtain the invention as specified in Claim 17.

With respect to **Claim 18**, Fisher teaches a speech processing board featuring a memory containing uniformly accessible language models and grammar rules as applied to Claim 1. Fisher also teaches the downloading of language models to an internal DSP memory, Col. 3, Lines 51-53. Fisher does not teach an audio processor that distributes

audio data to specific processor modules, however Walsh recites the host processor the distribution of audio data to specific DSPs, as applied to Claim 13.

Fisher and Walsh are analogous art because they are from a similar field of endeavor in speech processing in a network featuring multiple speech processing modules. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to combine the host processor for distributing audio data to specific DSPs as taught by Walsh with the speech processing board featuring a memory containing language models and grammar rules capable of being downloaded and stored to a local DSP memory as taught by Fisher to increase processing efficiency by distributing audio data to DSPs configured to handle a specific audio processing task, thus reducing necessary memory and increasing processing speed. Therefore, it would have been obvious to combine Walsh with Fisher for the benefit of obtaining a more efficient speech processing board by distributing audio data to specific DSPs, to obtain the invention as specified in Claim 18.

With respect to **Claim 19**, Fisher further discloses:

Collecting speech task results from said selected ones of said multiple processor modules; and *(call manager in a host system receiving notification of recognition results, Col. 3, Lines 59-63)*,

Forwarding collected speech task results to a host computer telephony (CT) system over a host communications bus *(media server featuring computer-based processing for a telephone application connected to a bus interface, Fig. 1, that receives recognition results via a speech task management function, Col. 3, Lines 59-63)*.

Claim 20 contains subject matter similar to Claim 18, and thus, is rejected for the same reasons. Also, it would have been obvious to one of ordinary skill in the art, at the time of invention, to implement the method of Claim 18 in a computer readable medium so as to provide increased method compatibility.

Claim 21 contains subject matter similar to Claim 19, and thus, is rejected for the same reasons.

8. **Claims 11 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher et al, in view of Kao et al *(U.S. Patent: 6,535,513)*

With respect to **Claim 11**, Fisher teaches the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus as applied to Claim 1. Fisher does not teach a communications bridge implemented in an FPGA, however Kao discloses:

A speech processing board, wherein said communications bridge is implemented in a field programmable gate array (FPGA) *(data switching apparatus and method utilizing an FPGA as a bus controller, Col. 10, Lines 64-65)*.

Fisher and Kao are analogous art because they are from a similar field of endeavor in network-based media applications. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to combine the switching apparatus and method containing an FPGA bus controller with the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus as taught by Fisher to implement a speech recognition control system with an FPGA as a communications bridge to offer further bus configuration capabilities. Therefore, it would have been obvious to combine

Kao with Fisher for the benefit of obtaining a multi-compatible, bus configurable speech recognition control system, to obtain the invention as specified in Claim 11.

With respect to **Claim 16,** Fisher teaches the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus as applied to Claim 1. Fisher does not teach a host system in the form of a VoIP gateway/endpoint, however Kao discloses:

A speech processing board, wherein said host system is a voice over IP (VoIP) gateway/endpoint *(switching apparatus capable of being used in a VoIP environment, Col. 4, Table 1).*

Fisher and Kao are analogous art because they are from a similar field of endeavor in network-based media applications. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to combine the switching apparatus for use over a VoIP network, thus providing VoIP compatibility, as taught by Kao, with the speech processing device containing multiple processors capable of accessing a language model and grammar database through a communications bus as taught by Fisher to implement a speech recognition control system with a the added ability of use in a practical VoIP network environment to increase system compatibility. Therefore, it would have been obvious to combine Kao with Everhart for the benefit of obtaining a configurable speech recognition control system for use in a practical VoIP environment, to obtain the invention as specified in Claim 16.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Phillips et al *(U.S. Patent: 6,249,761)*- teaches a speech recognition system utilizing a plurality of microprocessors and a shared memory.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James S. Wozniak whose telephone number is (703) 305-

8669 and email is James.Wozniak@uspto.gov. The examiner can normally be reached on Mondays-Fridays, 8:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached at (703) 305-4827. The fax/phone number for the Technology Center 2600 where this application is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology center receptionist whose telephone number is (703) 306-0377.

James S. Wozniak
8/23/2004

SUSAN MCFADDEN
PRIMARY EXAMINER